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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,614	11/24/2003	Martin G. Rammel	BO1-0162US	4243

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LEE & HAYES, PLLC
421 W. RIVERSIDE AVE.
SUITE 500
SPOKANE, WA 99201

EXAMINER	
DAO, THUY CHAN	
ART UNIT	**PAPER NUMBER**
2192	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,614	RAMMEL, MARTIN G.	
	Examiner	Art Unit	
	Thuy Dao	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *02/26/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to the application filed on November 24, 2003.

2. Claims 1-26 have been examined.

Information Disclosure Statement

3. The Office acknowledges receipt of the Information Disclosure Statement filed on February 26, 2004. It has been placed in the application file and the information referred to therein has been considered by the examiner.

Drawings

4. The drawings are objected to. In figure 1, out port "24" should be - -26- -.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

5. The specification is objected to because of minor informalities: acronyms CPU, FPGA, PCI, HDL, VHDL, FIFO, XST, BIT should be spelled out at the first appearance in the specification.

Claim Objections

6. Claims 3, 10, and 16 are objected to because of minor informalities: acronyms VHDL, FPGA, and FFT should be spelled out at the first appearance in claims.

6. Claim 7 is objected to. The phrase in line 3 should be - -adapted to [[deliniate]] delineate the portions ...- -.

Appropriate correction is required.

Claim Rejections – 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1-26 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,212,566 to Vanhoof et al. (hereinafter "Vanhoof").

Claim 1:

Vanhoof discloses an apparatus and *a method of performing a numerical simulation* (e.g., FIG. 7,col.21: 21-61), *comprising:*

programming a programmable device using a plurality of function blocks (e.g., col.6: 44-55; col.24: 25-28);

receiving input data (e.g., FIG. 8, col.21: 62 – col.22: 5);

providing a data path between a processor and the programmable device (e.g., col.21: 28-46);

performing a first portion of the numerical simulation on the processor (e.g., col.21: 62 – col.22: 19)*;*

performing a second portion of the numerical simulation on the programmable device (e.g., col.35: 32-43)*; and*

exchanging data from at least one of the first and second portions via the data path (e.g., col.21: 28-46; col.21: 62 – col.22: 5).

Claim 2:

The rejection of claim 1 is incorporated. Vanhoof also discloses *generating a plurality of function blocks* (e.g., col.24: 25-28).

Claim 3:

The rejection of claim 2 is incorporated. Vanhoof also discloses *generating a plurality of function blocks includes generating a plurality of VHDL function blocks* (e.g., col.6: 44-55).

Claim 4:

The rejection of claim 1 is incorporated. Vanhoof also discloses *exchanging data from at least one of the first and second portions via the data path includes providing inputs to a simulation block programmed into the programmable device from the processor via the data path* (e.g., col.21: 21-61).

Claim 5:

The rejection of claim 1 is incorporated. Vanhoof also discloses *exchanging data from at least one of the first and second portions via the data path includes providing outputs from a simulation block programmed into the programmable device to the processor via the data path* (e.g., FIG. 8, col.21: 62 – col.22: 5).

Claim 6:

The rejection of claim 1 is incorporated. Vanhoof also discloses *performing a second portion of the numerical simulation on the programmable device includes performing a portion of the original simulation on the programmable device* (e.g., FIG. 7, col. 21: 21-61).

Claim 7:

The rejection of claim 6 is incorporated. Vanhoof also discloses *performing a portion of the simulation on the programmable device includes: receiving inputs into a pair of gateway in blocks adapted to delineate the portions of the simulation to convert into VHDL for operation in hardware* (e.g., FIG. 1, col.11: 39 – col.12: 24).

Claim 8:

The rejection of claim 7 is incorporated. Vanhoof also discloses *performing a portion of the simulation on the programmable device includes: providing output from the programmable device* (e.g., FIG. 7, Evaluation Board #2, col.21: 21-61).

Claim 9:

The rejection of claim 8 is incorporated. Vanhoof also discloses *performing a portion of a simulation on the programmable device includes: coupling the outputs of the portion of the simulation to be run in hardware to at least one gateway out block adapted to delineate the extent of the code to be converted into VHDL for execution in hardware* (e.g., col.6: 44-55).

Claim 10:

The rejection of claim 1 is incorporated. Vanhoof also discloses *programming a programmable device includes programming a FPGA device* (e.g., col.24: 25-28).

Claim 11:

The rejection of claim 1 is incorporated. Vanhoof also discloses *receiving input data includes receiving first and second sine wave input data* (e.g., FIG. 1, col.11: 39 – col.12: 24).

Claim 12:

The rejection of claim 1 is incorporated. Vanhoof also discloses *forming a synthesis of the function blocks; and synthesizing a file adapted for use to program gate connections of the programmable device* (e.g., FIG. 2, col.12: 42-67).

Claims 13-15:

Claims 13-15 recite the same limitations as those of claims 1-5, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claims, it also teaches all of the limitations of claims 13-15.

Claim 16:

The rejection of claim 13 is incorporated. Vanhoof also discloses *programming a programmable device includes programming an FPGA device using at least some VHDL function blocks, and wherein performing a second portion of the numerical simulation on the programmable device includes performing an FFT on the programmable device* (e.g., FIG. 8, col.21: 62 – col.22: 5).

Claim 17:

The rejection of claim 16 is incorporated. Vanhoof also discloses limitations in claim 17 (e.g., col.10: 5-11).

Claim 18:

The rejection of claim 13 is incorporated. Vanhoof also discloses *forming a synthesis of the function blocks; and synthesizing a file adapted for use to program gate connections of the programmable device* (e.g., FIG. 2, col.12: 42-67).

Claim 19:

Claim 19 is an apparatus version, which recites the same limitations as those of claim 1, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claim, it also teaches all of the limitations of claim 19.

Claim 20:

The rejection of claim 19 is incorporated. Vanhoof also discloses *a generator adapted to generate a plurality of function blocks, at least some of the function blocks being adapted to perform a respective part of the second portion of the numerical simulation* (e.g., FIG. 7, Evaluation Board #2, col.21: 21-61).

Claim 21:

The rejection of claim 20 is incorporated. Vanhoof also discloses *the generator is further adapted to generate a plurality of VHDL function blocks* (e.g., col.6: 44-55).

Claim 22:

The rejection of claim 19 is incorporated. Vanhoof also discloses *the programmable device includes an FPGA device* (e.g., col.24: 25-28).

Claim 23:

The rejection of claim 19 is incorporated. Vanhoof also discloses *the input device is further adapted to receive input data* (e.g., FIG.1, col.11: 39 – col.12; 24).

Claim 24:

The rejection of claim 19 is incorporated. Vanhoof also discloses *the programmable device is further adapted to perform a simulation function block* (e.g., FIG. 8, col.21: 62 – col.22: 5).

Claim 25:

The rejection of claim 24 is incorporated. Vanhoof also discloses *the programmable device is further adapted to: receive inputs into a pair of gateway in* (e.g., col.21: 21-61).

Claim 26:

The rejection of claim 25 is incorporated. Vanhoof also discloses *the programmable device is further adapted to: provide output from the simulation block* (e.g., col.21: 62 – col.22: 5).

Claim Rejections – 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 13, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over "A Foundation Architecture For Elevating DSP in FPGAs" to Cantle et al., IDS document, Cite No. 1, published in 1999 (hereinafter "Cantle") in view of Admitted Prior Art (hereinafter "APA").

Claim 1:

Cantle discloses an apparatus *a method of performing a numerical simulation, comprising:*

a programmable device (e.g., page 6, Figure 5, FPGA component);

receiving input data (e.g., Figure 5, DIME I/O Connector, lines 14-16);

providing a data path between a processor and the programmable device (e.g., Figure 5, Parallel Communications Link, lines 14-18);

performing a first portion of the numerical simulation on the processor (e.g., Figure 5, SHARC digital signal processor DSP, lines 16-20);

performing a second portion of the numerical simulation on the programmable device; and exchanging data from at least one of the first and second portions via the data path (e.g., page 6, lines 10-20).

Cantle discloses a FPGA but does not explicitly disclose *programming a programmable device using a plurality of function blocks;*

However, in an analogous art, APA discloses *programming a programmable device using a plurality of function blocks* (e.g., page 5: 12-13 and page 6: 20-21).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to combine the teaching of APA into that of Cantle. One would have been motivated to do so to because said FPGA is programmable and re-programmable (FPGA stands for Field Programmable Gate Array, emphasis added).

Claims 13 and 19:

Claims 13 and 19 recite the same limitations as those of claim 1, wherein all claimed limitations have been addressed and/or set forth above. Therefore, as the reference teaches all of the limitations of the above claim, it also teaches all of the limitations of claims 13 and 19.

Conclusion

11. Any inquiry concerning this communication should be directed to examiner Thuy Dao (Twee), whose telephone is (571) 272 8570. The examiner can normally be reached on Monday, Tuesday, Thursday, and Friday from 6:00AM to 4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam, can be reached at (571) 272 3695.

The fax phone number for the organization where this application or proceeding is assigned is (571) 273 8300.

Any inquiry of a general nature of relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is (571) 272 2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T. Dao

TUAN DAM
SUPERVISORY PATENT EXAMINER